AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A distributed interconnect **between two separate substrates** comprising:

a first substrate;

a second substrate separate from said first substrate;

a first conductive transmission element **formed on said first substrate, said first conductive transmission element** disposed between a first and second terminal, said first conductive element having an impedance characteristic that increases from said first terminal to said second terminal~~, and~~ **;**

a second conductive transmission element **formed on said second substrate, said second conductive transmission element** disposed between a third and fourth terminal, said second conductive element having an impedance characteristic that increases from said third terminal to said fourth terminal, said first and second conductive transmission elements being positioned in parallel alignment with respect to each other; **[[and]]**

a plurality of conductive interconnect elements interconnecting said first and second transmission elements, said plurality of interconnect elements distributed along said first and second transmission elements and at least interconnecting said first terminal to said fourth terminal and interconnecting said second terminal to ~~said to~~ said third terminal; and

a first and second port, said first port connected to said first terminal and said second port connected to said third terminal.

2. (Original) The distributed interconnect according to claim 1, wherein said plurality of conductive interconnect elements includes at least one interconnect element evenly distributed between said first and second terminal and evenly distributed between said third and fourth terminal.

3. (Currently Amended) The distributed interconnect according to claim 1, wherein the impedance characteristic of said first and second conductive elements increases in ~~one of~~ a ~~stepped, tapered and~~ linear manner.

4. (Original) The distributed interconnect according to claim 1, said plurality of conductive interconnect elements positioned normal to said first and second transmission elements and in parallel with each other.

5. (Original) The distributed interconnect according to claim 4, said plurality of conductive interconnect elements evenly spaced from each other.

6. (Currently Amended) The distributed interconnect according to claim 1, said first conductive transmission element comprising a first metal trace disposed ~~on a first surface and~~ along a first edge of **[[a]]** **said** first substrate, and said second conductive transmission element comprising a second metal trace disposed ~~on a second surface and~~ along a second edge of **[[a]]** **said** second substrate, said first edges and second edges laterally positioned next to each other forming a parallel gap therebetween.

7. (Original) The distributed interconnect according to claim 6, said plurality of conductive interconnect elements comprising equally spaced bondwires spanning the gap in a laterally parallel and equally space configuration.

8. (Currently Amended) The distributed interconnect according to claim 6, said first and second traces having ~~one of~~ a tapered ~~and stepped~~ shape **having no steps**.

9. (Withdrawn) The distributed interconnect according to claim 6, further comprising a bilateral trace electrically connected to an upper side of said first and second traces, said first and second traces having one of a dual stepped and dual tapered shape.

10. (Withdrawn) The distributed interconnect according to claim 1, said first conductive transmission element comprising a first metal trace disposed on an upper surface of a substrate, and said second conductive transmission element comprising a second metal trace disposed on a lower surface of said substrate, said first and second traces being partially positioned above one another in a parallel orientation.

11. (Withdrawn) The distributed interconnect according to claim 10, said plurality of conductive interconnect elements comprising a plurality of one of metal filled and edge plated vias disposed through said upper and lower surface of said substrate.

12. (Withdrawn) The distributed interconnect according to claim 10, said first and second metal traces having one of a tapered, stepped, dual tapered, and dual stepped configuration.

13. (Withdrawn) The distributed interconnect according to claim 1, said first conductive transmission element comprising a first lead connected to a device disposed internally in a semiconductor package, and said second conductive transmission element comprising a second lead externally disposed on a surface of a substrate.

14. (Withdrawn) The distributed interconnect according to claim 13, said plurality of conductive interconnect elements comprising a plurality of one of metal filled and edge plated vias disposed internally in the semiconductor package.

15. (Withdrawn) The distributed interconnect according to claim 14, further comprising a respective plurality of terminal leads exiting said package, said terminal leads having an internal end and an external end, wherein said plurality of vias are bonded to each respective terminal lead, and said external leads are bonded to said second lead.

16. (Withdrawn) The distributed interconnect according to claim 15, said first and second lead having a pillar shape in which pads of equal area are provided for each interconnect element and pillar portions interconnect said pads, and wherein a width of said pillar portions are incrementally decreased from said first terminal to said second terminal and from said third terminal to said fourth terminal.

17. (Withdrawn) The distributed interconnect according to claim 15, said first and second lead having one of a tapered and stepped shape.

18. (Currently Amended) A method for interconnecting electrical components **between two separate substrates** which minimizes coupling inductance and increases bandwidth, the method comprising:

disposing a first conductive transmission element between a first and second terminal **on a first substrate**, the first conductive element having an impedance characteristic that increases from the first terminal to the second terminal,

disposing a second conductive transmission element between a third and fourth terminal **on a second substrate**, the second conductive element having an impedance characteristic that increases from said third terminal to the fourth terminal, and

positioning the first and second conductive elements in parallel alignment with respect to each other;

interconnecting a plurality of conductive interconnect elements between the first and second transmission elements by,

distributing the plurality of interconnect elements along the first and second transmission elements,

at least interconnecting the first terminal to the fourth terminal, and

at least interconnecting the second terminal to the to the third terminal; and

electrically connecting a first port to the first terminal, and

electrically connecting a second port to the third terminal.

19. (Currently Amended) The method according to claim 1**8**, further comprising evenly distributing the plurality of conductive interconnect elements between the first and second terminal and between the third and fourth terminal.

20. (Currently Amended) The method according to claim 1**8**, further comprising increasing the impedance characteristic of the first and second conductive elements in ~~one of~~ a ~~stepped, tapered and~~ linear manner.

21. (Currently Amended) The method according to claim 1**8**, further comprising positioning the plurality of conductive interconnect elements normal to the first and second transmission elements and in a lateral and parallel orientation with respect to each other.

22. (Currently Amended) The method according to claim **[[1]] 20**, further comprising,

forming the first conductive transmission element from a first metal trace,

disposing the first metal trace on a first surface and along a first edge of **[[a]] the** first substrate,

forming the second conductive transmission element from a second metal trace,

disposing the second metal trace on a second surface and along a second edge of **[[a]] the** second substrate, and

positioning the first edges and second edges laterally next to each other to form a parallel gap therebetween.

23. (Original) The method according to claim 22, further comprising utilizing equally spaced bondwires spanning the parallel gap as the plurality of conductive interconnect elements.

24. (Currently Amended) The method according to claim 22, further comprising providing first and second traces which have ~~one of~~ a tapered ~~and stepped~~ shape **having no steps**.

25. (Withdrawn) The method according to claim 22, further comprising electrically connecting a bilateral trace to an upper side of the first and second traces, wherein the first and second traces have one of a dual stepped and dual tapered shape.

26. (Withdrawn) The method according to claim 18, further comprising,

forming the first conductive transmission element from a first metal trace,

disposing the first metal trace on an upper surface of a substrate,

forming the second conductive transmission element from a second metal trace,

disposing the second metal trace on an upper surface of a substrate, and

positioning the first and second traces partially above one another in a parallel orientation.

27. (Withdrawn) The method according to claim 26, further comprising utilizing a plurality of one of metal filled and edge plated vias disposed through the upper and lower surface of the substrate as the plurality of conductive interconnect elements.

28. (Withdrawn) The method according to claim 26, further comprising providing first and second metal traces having one of a tapered, stepped, dual tapered, and dual stepped configuration.

29. (Withdrawn) The method according to claim 18, further comprising,

utilizing a first lead connected to a device disposed internally in a semiconductor package as the first conductive transmission element, and

utilizing a second lead externally disposed on a surface of a substrate as the second conductive transmission element.

30. (Withdrawn) The method according to claim 29, utilizing a plurality of one of metal filled and edge plated vias disposed internally in the semiconductor package as the plurality of conductive interconnect elements interconnecting the first and second conductive leads.

31. (Withdrawn) The method according to claim 30, further comprising,

utilizing a respective plurality of terminal leads for exiting the package, wherein the terminal leads have an internal end and an external end,

electrically connecting the at least one via to each respective terminal lead, and

electrically connecting the external leads to the second lead.

32. (Withdrawn) The method according to claim 31, further comprising providing a first and second lead having a stacked pillar shape in which pads of equal area are provided for each interconnect element and pillar portions interconnect the pads, and wherein a width of the pillar portions are incrementally decreased from said first terminal to said second terminal and from said third terminal to said fourth terminal.

33. (Withdrawn) The method according to claim 31, further comprising utilizing a first and second lead having one of a tapered and stepped shape.

34. (New) A distributed interconnect between two separate substrates comprising:

a first conductive transmission element formed from a first tapered trace disposed on a first substrate, said first trace having at least a first and second terminal and having an impedance characteristic that linearly increases from said first terminal to said second terminal;

a second conductive transmission element formed from a second tapered trace disposed on a second substrate, said second trace having at least a third and fourth terminal and having an impedance characteristic that linearly increases from said third terminal to said fourth terminal;

a plurality of conductive interconnect elements interconnecting said first and second transmission elements-and at least interconnecting said first terminal to said fourth terminal and said second terminal to said third terminal; and

a first and second I/O port for outside electrical communication, said first port in communication with said second terminal and said second port in communication with said fourth terminal.

35. (New) The distributed interconnect according to claim 34, wherein said plurality of conductive interconnect elements are evenly spaced and distributed between said first and second terminals and evenly spaced and distributed between said third and fourth terminals.

36. (New) The distributed interconnect according to claim 34, each of said first and second tapered traces comprising a base side, a tapered side having no steps which opposes said base side at an inclined angle, a short side normal to said base side which connects to both said base and a most inclined end of said tapered side, said short side being positioned proximate and outside one of said first or third terminals, and another portion of said first and second trace opposing said short side which interconnects said base side and a most upwardly

inclined end of said tapered side, said portion positioned proximate and outside of said second or fourth terminals and having a width greater than that of said short side.

37. (New) The distributed interconnect according to claim 36, said plurality of conductive interconnect elements positioned normal to said base sides of said first and second tapered traces and further in lateral and parallel orientation with respect to each other.

38. (New) The distributed interconnect according to claim 36, said first and second ports comprising said portions of said first and second tapered traces which oppose said short sides and which interconnects the base side and the most upwardly inclined end of said tapered side, and of which are positioned proximate and outside said second or fourth terminals.

39. (New) The distributed interconnect according to claim 36 , said base side of said first trace disposed along a first edge of said first substrate, and said base side of said second trace disposed along a second edge of said second substrate, said first and second edges laterally positioned next to each other forming a generally parallel gap therebetween.

40. (New) The distributed interconnect according to claim 34, said plurality of conductive interconnect elements comprising equally spaced bondwires spanning the gap in a lateral and parallel orientation with respect to each other.

41. (New) A method for interconnecting electrical components between two substrates which minimizes coupling inductance and increases bandwidth, the method comprising:

disposing a first conductive transmission element formed from a first tapered trace on a first substrate, the first trace having at least a first and second terminal and having an impedance characteristic that increases linearly from the first terminal to the second terminal;

disposing a second conductive transmission element formed from a second tapered trace on a second substrate, the second trace having at least a third and fourth terminal and having an impedance characteristic that increases linearly from the third terminal to the fourth terminal;

interconnecting a plurality of conductive interconnect elements between the first and second transmission elements by, evenly spacing and distributing the plurality of interconnect elements between the first and second terminals and between the third and

fourth terminals, at least interconnecting the first terminal to the fourth terminal, and at least interconnecting the second terminal to the to the third terminal;

providing a first I/O port for outside electrical communication positioned proximate and outside the second terminal; and

providing a second I/O port for outside electrical communication positioned proximate and outside the fourth terminal.

42. (New) The method according to claim 41, each of the first and second tapered traces comprising a base side, a tapered side having no steps which opposes the base side at an inclined angle, a short side normal to the base side which connects to both of the base and tapered sides, the short side being positioned proximate and outside one of the first or third terminals, and another portion of said first and second trace opposing the short side which interconnects the base side and a most upwardly inclined end of said tapered side, the portion positioned proximate and outside the second or fourth terminals and having a width greater than that of the short side.

43. (New) The method according to claim 42, further comprising positioning the plurality of conductive interconnect elements normal to the base sides of the first and second tapered traces and in a lateral and parallel orientation with respect to each other.

44. (New) The method according to claim 42, further comprising,

disposing the base side of the first trace along a first edge of the first substrate;

disposing the base side of the second trace along a second edge of the second substrate; and

positioning the first and second edges laterally next to each other to form a parallel gap therebetween.

45. (New) The method according to claim 22, further comprising utilizing equally spaced bondwires spanning the parallel gap as the plurality of conductive interconnect elements.